MAXIM

CMOS Quad, Serial Interface, 8-Bit D/A Converter

General Description

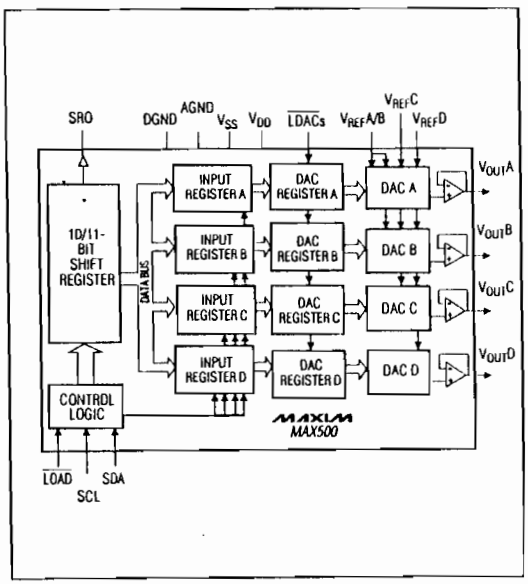
MAX500 is a quad 8-bit voltage output digital to analog converter (DAC) with a cascadable serial interface. The MAX500 circuit includes four output buffer amplifiers and input logic for an easy-to-use two- or three-wire serial interface. In a system with several MAX500s, only one serial data line is required to load all the DACs by cascading them. The MAX500 contains double-buffered logic and a 10-bit shift register which allows all four DACs to be updated simultaneously using one control signal. There are three reference inputs so that the range of two of the DACs can be independently set while the other two DACs track each other.

The MAX500 achieves 8-bit performance over the full operating temperature ranges without external trimming.

Applications

Minimum Component Count Analog Systems
Digital Offset/Gain Adjustment
Industrial Process Control
Arbitrary Function Generators
Automatic Test Equipment

Functional Block Diagram



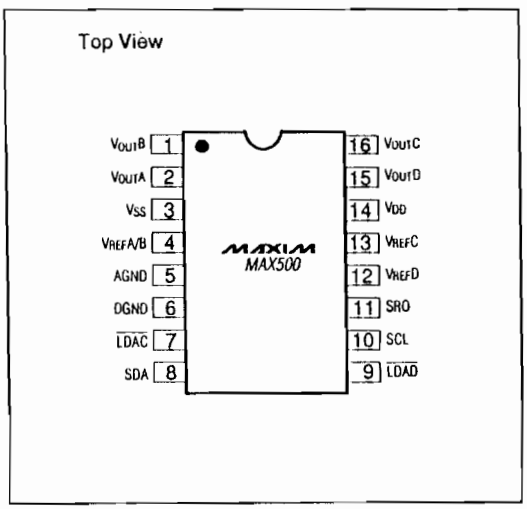
Features

- ♦ Buffered Voltage Outputs
- ♦ Double-Buffered Digital Inputs
- ♦ Microprocessor and TTL/CMOS Compatible
- ♦ Requires No External Adjustments
- ♦ Two- or Three-Wire Cascadable Serial Interface
- ♦ 16-Pin Package
- ♦ Operates from Single or Dual Supplies

Ordering Information

PART	TEMP. RANGE	PACKAGE	ERROR
MAX500ACPE	0°C to +70°C	Plastic DIP	±1 LSB
MAX500BCPE	0°C to +70°C	Plastic DIP	±2 LSB
MAX500ACWE	0°C to +70°C	Wide SO	±1 LSB
MAX500BCWE	0°C to +70°C	Wide SO	±2 LSB
MAX500BC/D	0°C to +70°C	Dice	±2 LSB
MAX500AEWE	-40°C to +85°C	Wide SO	±1 LSB
MAX500BEWE	-40°C to +85°C	Wide SO	±2 LSB
MAX500AEJE	-40°C to +85°C	CERDIP	±1 LSB
MAX500BEJE	-40°C to +85°C	CERDIP	±2 LSB
MAX500AMJE	-55°C to +125°C	CERDIP	±1 LSB
MAX500BMJE	-55°C to +125°C	CERDIP	±2 LSB

Pin Configuration



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ABSOLUTE MAXIMUM RATINGS

V_{DD} to AGND ..... -0.3V, +17V
V_{DD} to DGND ..... -0.3V, +17V
V_{SS} to DGND ..... -7V, V_{DD} +0.3V
V_{DD} to V_{SS} ..... -0.3V, +24V
Digital Input Voltage to DGND ..... -0.3V, V_{DD} +0.3V
V_{REF} to AGND ..... -0.3V, V_{DD} +0.3V
V_{OUT} to AGND (Note 1) ..... -0.3V, V_{DD} +0.3V

Power Dissipation (any package) to +75°C 500mW
Derate Above +75°C ..... 8mW/°C
Operating Temperature Range
MAX500XC ..... 0°C to +70°C
MAX500XE ..... -40°C to +85°C
MAX500XM ..... -55°C to +125°C
Storage Temperature ..... -65°C to +150°C
Lead Temperature (soldering 10 sec.) ..... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS: Dual Supply Specifications

(V_{DD} = +11.4V to +16.5V, V_{SS} = -5V ±10%, AGND = DGND = 0V, V_{REF} = +2V to (V_{DD} - 4V), T_A = T_{MIN} to T_{MAX} unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STATIC PERFORMANCE							
Resolution				8			Bits
Total Unadjusted Error		V_{DD} = 15V ±5% V_{REF} = 10V	MAX500A MAX500B			±1 ±2	LSB
Relative Accuracy		MAX500A MAX500B				±½ ±1	LSB
Differential Nonlinearity Guaranteed Monotonic						±1	LSB
Full Scale Error		MAX500A MAX500B				±½ ±1	LSB
Full Scale Tempco		V_{REF} = 10V			±5	•	ppm/°C
Zero Code Error		T_A = 25°C	MAX500A MAX500B			±15 ±20	mV
		T_A = T_{MIN} to T_{MAX}	MAX500A MAX500B			±20 ±30	
Zero Code Tempco					±30		µV/°C
REFERENCE INPUT							
Reference Input Range				2		V_{DD} - 4	V
Reference Input Resistance Pins 12, 13 Reference Input Resistance Pin 4				11 5.5			kΩ
Reference Input Capacitance		(Note 2) Code Dependent				100	pF
Channel-to-Channel Isolation		(Note 3)		-60			dB
AC Feedthrough		(Note 3)		-70			dB
DIGITAL INPUTS							
Digital Input High Voltage	V_{IH}			2.4			V
Digital Input Low Voltage	V_{IL}					0.8	V
Digital Output High Voltage	V_{OH}	I_{OUT} = -1mA, SRO only		V_{DD} -1			V
Digital Output Low Voltage	V_{OL}	I_{OUT} = 1mA, SRO only		0.4			V

ELECTRICAL CHARACTERISTICS: Dual Supply Specifications (continued)

(V_{DD} = +11.4V to +16.5V, V_{SS} = -5V ±10%, AGND = DGND = 0V, V_{REF} = +2V to (V_{DD} - 4V), T_A = T_{MIN} to T_{MAX} unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Digital Input Leakage Current		(Note 4)	Excluding LOAD LOAD = 0V			±1 30	µA
Digital Input Capacitance		(Note 5)				8	pF
DYNAMIC PERFORMANCE							
Voltage Output Slew Rate		(Note 5)		3			V/µs
V_{OUT} Settling Time		To ±½ LSB, V_{REF} = 10V, V_{DD} = +15V, 2kΩ in parallel with 100pF load				4	µs
Digital Feedthrough		(Note 6)			50		nV-s
Digital Crosstalk		(Note 6)			50		nV-s
Output Load Resistance		V_{OUT} = 10V		2			kΩ
POWER SUPPLIES							
Positive Supply Voltage	V_{DD}	For specificed performance		11.4		16.5	V
Positive Supply Current	I_{DD}	Outputs unloaded.	T_A = 25°C T_A = T_{MIN} to T_{MAX}			10 12	mA
Negative Supply Current	I_{SS}	Outputs unloaded.	T_A = 25°C T_A = T_{MIN} to T_{MAX}			-9 -10	mA
SWITCHING CHARACTERISTICS (Note 5)							
THREE-WIRE MODE							
SDA Valid to SCL Setup	t_{S1}			150			ns
SDA Valid to SCL Hold	t_{H1}			0			ns
SCL High Time	t_1			350			ns
SCL Low Time	t_2			350			ns
$\overline{LOAD}$ Pulse Width	t_{LDW}			150			ns
$\overline{LOAD}$ Delay from SCL	t_{LDS}			150			ns
$\overline{LDAC}$ Pulse Width	t_{LOAC}			150			ns
SRO Output Delay	t_{D1}	C_{LOAD} = 50pF				150	ns
TWO-WIRE MODE							
SDA Valid to SCL Hold	t_{H1}			0			ns
SCL High Time	t_1			350			ns
SCL Low Time	t_2			350			ns
$\overline{LDAC}$ Pulse Width	t_{LOAC}			150			ns
SCL Valid to SDA Setup	t_{S1}	(Start condition)		150			ns
SDA Valid to SCL Setup	t_{S2}	(Stop condition)		100			ns
SDA Valid to Rising SCL	t_{S3}			125			ns
SRO Output Delay	t_{D1}	C_{LOAD} = 50pF				150	ns

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ELECTRICAL CHARACTERISTICS: Single Supply Specifications

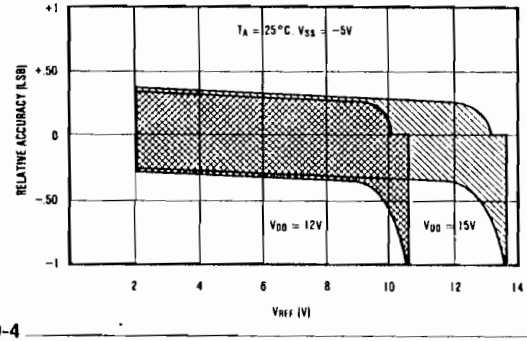
(V_{DD} = +15V ±5%, V_{SS} = AGND = DGND = 0V, V_{REF} = 10V, T_A = T_{MIN} to T_{MAX} unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STATIC PERFORMANCE							
Resolution				8			Bits
Total Unadjusted Error		V_{DD} = 15V ±5% V_{REF} = 10V	MAX500A MAX500B			±1 ±2	LSB
Relative Accuracy			MAX500A MAX500B			±½ ±1	LSB
Differential Nonlinearity Guaranteed Monotonic						±1	LSB
Full Scale Error			MAX500A MAX500B			±½ ±1	LSB
Full Scale Tempco		V_{REF} = 10V			±5		ppm/°C
Zero Code Error		T_A = 25°C	MAX500A MAX500B			±15 ±20	mV
		T_A = T_{MIN} to T_{MAX}	MAX500A MAX500B			±20 ±30	mV
Zero Code Tempco					±30		µV/°C
REFERENCE INPUT – All specifications are the same as for dual supplies.							
DIGITAL INPUTS – All specifications are the same as for dual supplies.							
DYNAMIC PERFORMANCE – All specifications are the same as for dual supplies.							
POWER SUPPLIES							
Positive Supply Voltage	V_{DD}	For specified performance		14.25		15.75	V
Positive Supply Current	I_{DD}	Outputs Unloaded T_A = 25°C T_A = T_{MIN} to T_{MAX}				10 12	mA
SWITCHING CHARACTERISTICS – All specifications are the same as for dual supplies.							

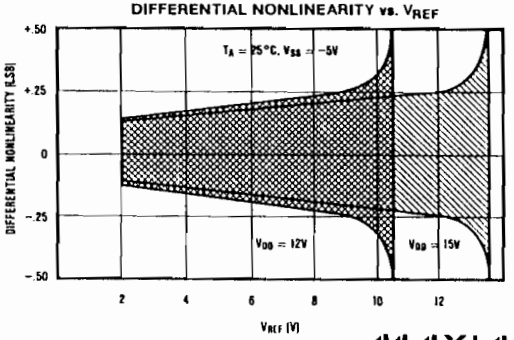
Note 1: The outputs may be shorted to AGND provided that the power dissipation of the package is not exceeded. Typical short circuit current to AGND is 25mA.
Note 2: Guaranteed by design. Not production tested.
Note 3: V_{REF} = 10 kHz, 10V peak-to-peak sine wave.
Note 4: $\overline{LOAD}$ has a weak internal pull-up resistor to V_{DD}.
Note 5: Sample tested at +25°C to ensure compliance.
Note 6: DAC switched from all 1s to all 0s, and all 0s to all 1s code.

Typical Operating Characteristics

RELATIVE ACCURACY vs. V_{REF}



DIFFERENTIAL NONLINEARITY vs. V_{REF}



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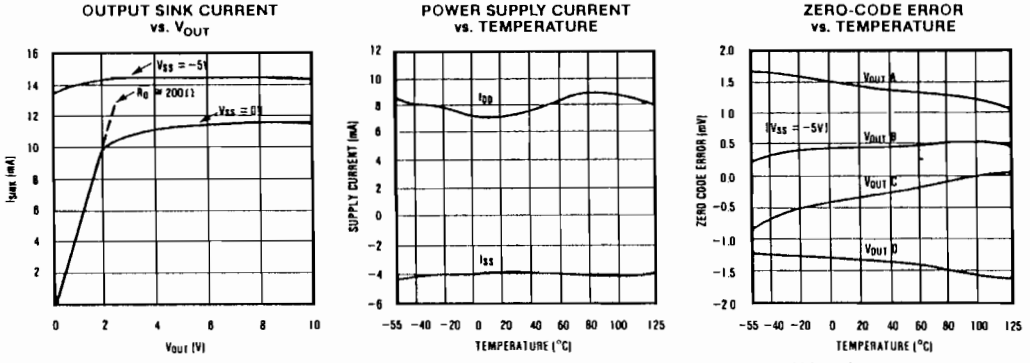
Typical Operating Characteristics (Continued)



Detailed Description

The MAX500 has four matched voltage output digital-to-analog converters (DAC). The DACs are "inverted" R-2R ladder networks which convert 8 digital bits into equivalent analog output voltages in proportion to the applied reference voltage(s). Two DACs in the MAX500 have a separate reference input while the other two DACs share one reference input. A simplified circuit diagram of one of the four DACs is provided in Figure 1.

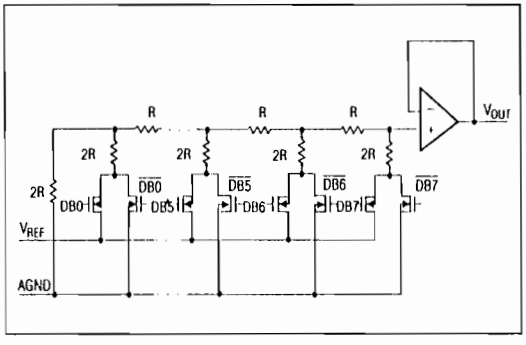


Figure 1. Simplified DAC Circuit Diagram

VREF Input

The voltage at V_{REF} pins (pins 4, 12 and 13) sets the full scale output of the DAC. The input impedance of the V_{REF} inputs is code dependent. The lowest value, approximately 11kΩ (5.5kΩ for pin 4), occurs when the input code is 01010101. The maximum value of infinity occurs when the input code is 00000000. Because the input resistance at V_{REF} is code dependent, the DAC's reference sources should have an output impedance of no more than 20Ω (no more than 10Ω for pin 4). The input capacitance at V_{REF} is also code dependent and typically varies from 15pF to 35pF (30pF to 70pF for pin 4).

$V_{OUT}A$, $V_{OUT}B$, $V_{OUT}C$, and $V_{OUT}D$ can be represented by a digitally programmable voltage source as:

$$V_{OUT} = N_b \times \frac{V_{REF}}{256}$$

where N_b is the numeric value of the DAC's binary input code.

Output Buffer Amplifiers

All voltage outputs are internally buffered by precision unity gain followers which slew at greater than 3V/µs. When driving 2kΩ in parallel with 100pF with a full scale transition (0V to +10V or +10V to 0V), the output settles to ±½ LSB in less than 4µs. The buffers will also drive 2kΩ in parallel with 500pF to 10V levels without oscillation. Typical dynamic response and settling performance of the MAX500 is shown in Figures 2 and 3.

A simplified circuit diagram of an output buffer is shown in Figure 4. Input common mode range to AGND is provided by a PMOS input structure. The output circuitry incorporates a pull-down circuit to actively drive V_{OUT} to within +15mV of the negative supply (V_{SS}). The buffer circuitry allows each DAC output to sink, as well as source up to 5mA. This is especially important in single supply applications, where V_{SS} is connected to AGND, so that the zero error is kept at or under ½ LSB (V_{REF} = +10V). A plot of the output sink current versus output voltage is shown in the Typical Operating Characteristics section.

Digital Inputs and Interface Logic

The digital inputs are compatible with both TTL and 5V CMOS logic, however, the power supply current (I_{DD}) is somewhat dependent on the input logic level. Supply current is specified for TTL input levels (worst case) but is reduced (by about 150µA) when the logic inputs are driven near DGND or 4 volts above DGND.

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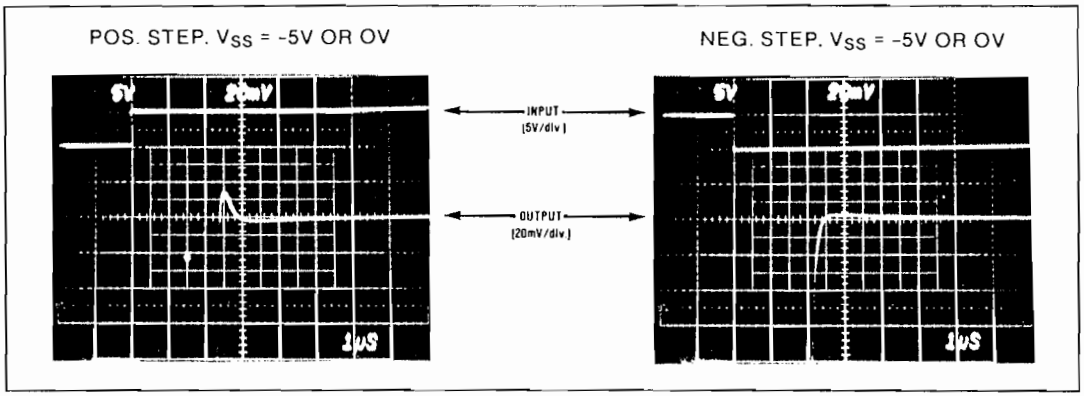

Figure 2. Positive and Negative Settling Times, V_{SS} = 0V or -5V

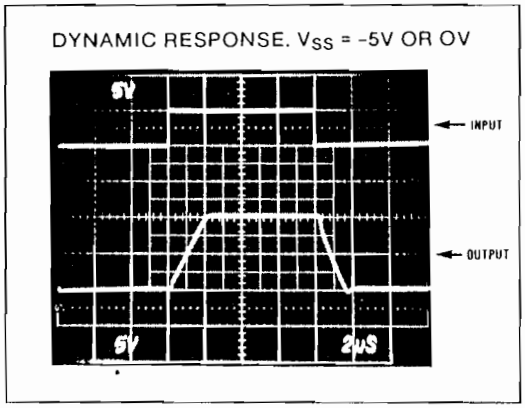

Figure 3. Dynamic Response, V_{SS} = 0V or -5V

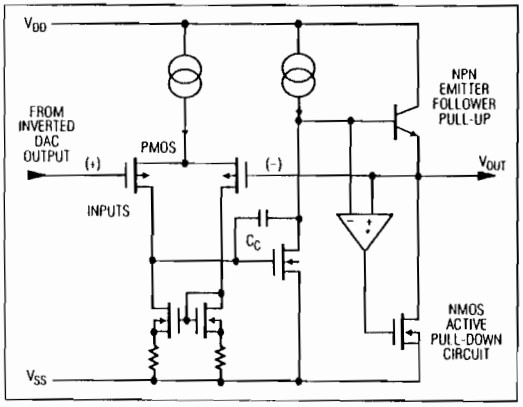

Figure 4. Simplified Output Buffer Circuit

The MAX500 allows the user to choose between a three-wire serial interface and a two-wire serial interface. The choice between the two-wire and the three-wire interface is set by the LOAD signal. If the LOAD is allowed to float (it has a weak internal pull-up resistor to V_{DD}), the two-wire interface is selected. If the LOAD signal is kept to a TTL logical high level, the three-wire interface is selected.

Three-Wire Interface

The three-wire interface uses the classic Serial Data (SDA), Serial Clock (SCL), and LOAD signals used in standard shift registers. The data is clocked in on the falling edge of SCL until all 10 bits (8 data bits and 2 address bits) are entered into the SHIFT REGISTER. A low level on LOAD line initiates the transfer of data from the SHIFT REGISTER to the addressed INPUT REGISTER. The data can stay in this register until all four of the INPUT REGISTERs are updated. Then all of the DAC REGISTERs can be simultaneously updated using the LDAC (LOAD DAC) signal. When LDAC is low, the INPUT REGISTER's data is loaded into the DAC REGISTERs (see Figure 5 for timing diagram). This mode is cascadable by connecting Serial Output (SRO) to the second chip's SDA pin. The delay of the SRO pin from SCL does not cause setup/hold time violations no matter how many MAX500s are cascaded.

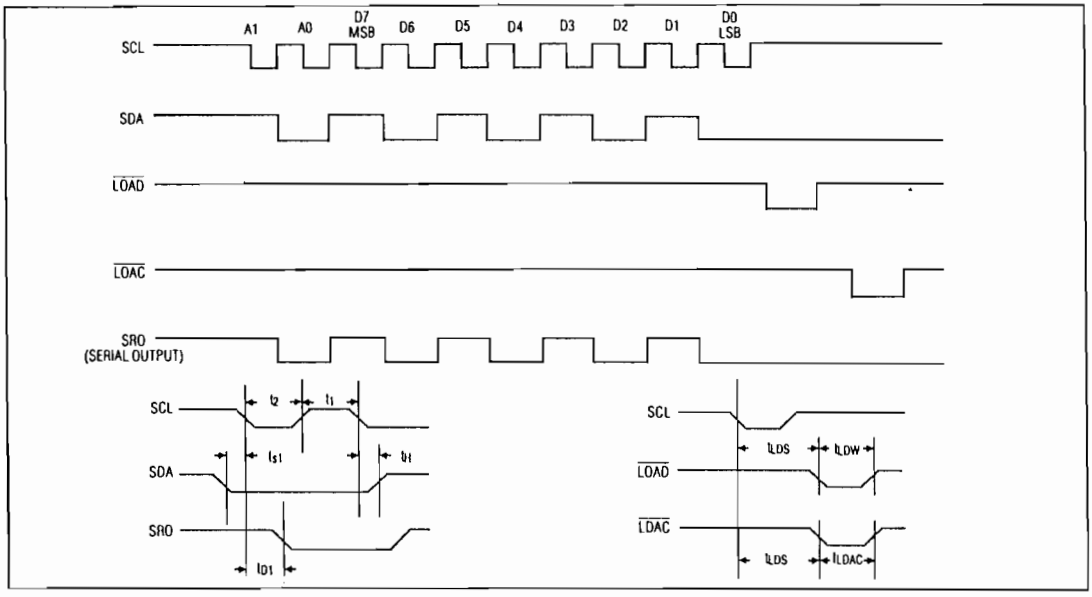

Figure 5. 3-Wire Mode

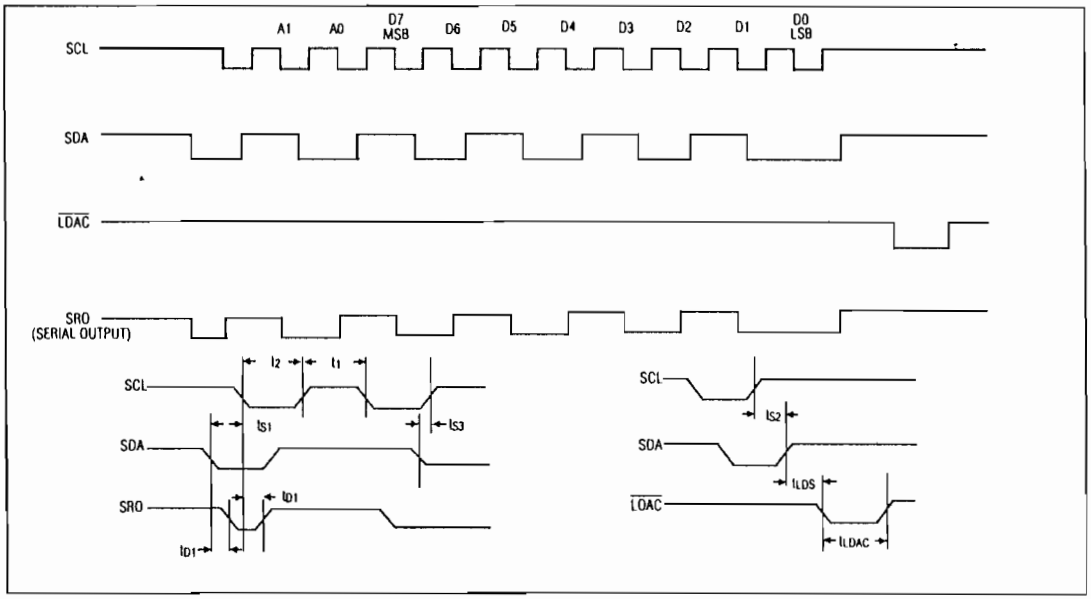

Figure 6. 2-Wire Mode

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Two-Wire Interface

The two-wire interface uses SDA and SCL only. $\overline{LOAD}$ must be floating or tied to V_{DD}. Each data frame (8 data bits and 2 address bits) is synchronized by a timing relationship between SDA and SCL (see Figure 6 for the timing diagram). Both SDA and SCL should normally be high when inactive. A falling edge of SDA (while SCL is high) followed by a falling edge of SCL (while SDA is low) is the start condition. This always loads a 0 into the first bit of the SHIFT REGISTER. The SHIFT REGISTER is extended to 11 bits so this "data" will not affect the INPUT REGISTER information. The timing now follows the three-wire interface except the SDA line is not allowed to change when SCL is high (this prevents the MAX500 from retriggering its start condition). After the last data bit is entered, the SDA line should go low (while the SCL line is low), then the SCL line should rise followed by the SDA line rising. This is defined as the stop condition, or end of frame.

Cascading the two-wire interface can be done, but the user must be careful of both timing and formatting. Timing must take into account the intrinsic delay of the SRO pin from the internally generated start/stop conditions. The t_{S2} value should be increased by n times t_{D1}, (where n = number of cascaded MAX500s). The t_{LDS} value should also be increased by n times t_{D1}. No other timing parameters need to be modified. A more serious concern is one of formatting. Generally since each frame has a start/stop condition, each chip that has data cascaded through it will accept that data as if it were its own data. Therefore, to circumvent this limitation, the user should not generate a stop bit until all DACs have been loaded. For example, if there are three MAX500s cascaded in the two-wire mode, the data transfer should begin with a start condition, then followed by 10 data bits, a zero bit, 10 data bits, a zero bit, 10 data bits, and then a stop condition. This will prevent each MAX500 from decoding the middle data for itself.

The data is entered into the SHIFT REGISTER in the following order:

A1 A0 D7 D6 D5 D4 D3 D2 D1 D0
(First) (MSB) (Last)

where address bits A1 and A0 select which DAC register receives data from the internal SHIFT REGISTER. Table 1 lists the channel addresses. D7 through D0 (D7 is MSB) is the data byte.

Table 1. DAC Addressing

A1	A0	SELECTED INPUT REGISTER
L	L	DAC A Input Register
L	H	DAC B Input Register
H	L	DAC C Input Register
H	H	DAC D Input Register

Since $\overline{LDAC}$ is asynchronous with respect to SCL, SDA, and LOAD, care must be taken to assure that incorrect data is not latched through to the DAC REGISTERs. If the three-wire serial interface is used, $\overline{LDAC}$ can be tied low permanently or $\overline{LDAC}$ can be tied to $\overline{LOAD}$ as long as t_{LDS} is always maintained. However, if the two-wire interface is used, $\overline{LDAC}$ should not fall before the stop condition is internally detected. (This is the reason for the t_{LDS} delay of $\overline{LDAC}$ after the last rising edge of SDA.)

The SRO output swings from V_{DD} to DGND. Cascading to other MAX500s poses no problem. If SRO is used to drive a TTL compatible input, then a clamp diode between TTL +5V and V_{DD} and current limiting resistor should be used. This will prevent potential latchup problems with the 5V supply.

Table 2 shows the truth table for SDA, SCL, $\overline{LOAD}$, and $\overline{LDAC}$ operation. Figures 5 and 6 show the timing diagrams for the MAX500.

Table 2. Logic Input Truth Table

SCL	SDA	$\overline{LOAD}$	$\overline{LDAC}$	FUNCTION
F	Data	V_{DD}	H	Latching data into Shift Register (2W)
H	Data	V_{DD}	H	Data should not be changing (2W)
L	X	V_{DD}	H	Data is allowed to change (2W)
F	Data	M	H	Latching data into Shift Register (3W)
H	X	M	H	Data is allowed to change (3W)
L	X	M	H	Data is allowed to change (3W)
H	X	L	H	Loads Input Register from Shift Register (3W)
H	X	L	L	DAC register reflects data held in their respective Input Registers

Notes:

H = Logical High
L = Logical Low
M = TTL Logical High
X = Don't Care
2W = 2-Wire
3W = 3-Wire
F = Falling Edge

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Applications Information

Power Supply and Reference Operating Ranges

The MAX500 is fully specified to operate with V_{DD} between +12V ± 5% and +15V ±10% (+11.4V to +16.5V), and with V_{SS} from 0V to -5.5V. 8-bit performance is also guaranteed for single supply operation (V_{SS} = 0V), however, zero code error is reduced when V_{SS} is -5V (see Output Buffer Amplifier section).

For adequate DAC and buffer operating range, the V_{REF} voltage must always be at least 4V below V_{DD}. The MAX500 is specified to operate with a reference input range of +2V to V_{DD} - 4V.

Ground Management

Digital or AC transient signals between AGND and DGND will create noise at the analog outputs. It is recommended that AGND and DGND be tied together at the DAC and that this point be tied to the highest quality ground that is available. If separate ground busses are used, then two clamp diodes (1N914 or equivalent) should be connected between AGND and DGND to keep the two ground busses within one diode drop of each other. To avoid parasitic device turn-on, AGND must not be allowed to be more negative than DGND. DGND should be used as supply ground for bypassing purposes.

Careful PCB ground layout techniques should be used to minimize crosstalk between DAC outputs, the reference input(s), and the digital inputs. This is particularly important if the reference is driven from an AC source. Figure 7 shows suggested circuit board layouts for minimizing crosstalk.

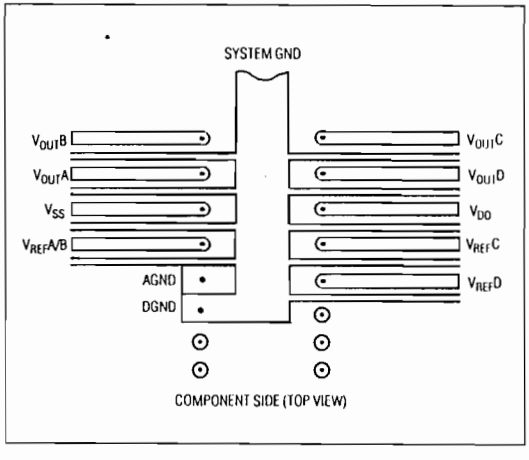

Figure 7. Suggested MAX500 PCB Layout for Minimizing Crosstalk

Unipolar Output

In unipolar operation, the output voltages and the reference input(s) are the same polarity. Unipolar circuit configuration is shown in Figure 8 for the MAX500. The device can be operated from a single supply with a slight increase in zero error (see Output Buffer Amplifier section). To avoid parasitic device turn-on, the voltage at V_{REF} must always be positive with respect to AGND. The unipolar code table is given in Table 3.

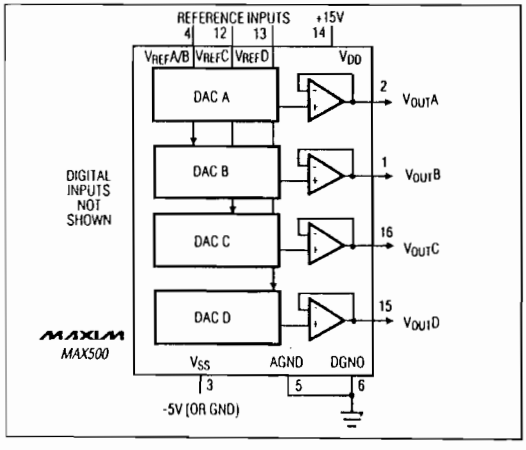

Figure 8. MAX500 Unipolar Output Circuit

Table 3. Unipolar Code Table

MSB				DAC CONTENTS			LSB	ANALOG OUTPUT
1	1	1	1	1	1	1	1	$+V_{REF}\left(\frac{255}{256}\right)$
1	0	0	0	0	0	0	1	$+V_{REF}\left(\frac{129}{256}\right)$
1	0	0	0	0	0	0	0	$+V_{REF}\left(\frac{128}{256}\right) = +\frac{V_{REF}}{2}$
0	1	1	1	1	1	1	1	$+V_{REF}\left(\frac{127}{256}\right)$
0	0	0	0	0	0	0	1	$+V_{REF}\left(\frac{1}{256}\right)$
0	0	0	0	0	0	0	0	0V

Note: 1 LSB = $(V_{REF})(2^{-8}) = +V_{REF}\left(\frac{1}{256}\right)$

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Bipolar Output

Each DAC output may be configured for bipolar operation using the circuit in Figure 9. One op-amp and two resistors are required per channel. With R1 = R2:

$$V_{OUT} = V_{REF}(2D_A - 1)$$

where D_A is a fractional representation of the digital word in Register A.

Table 4 shows the digital code versus output voltage for the circuit in Figure 9.

Table 4. Bipolar Code Table

DAC CONTENTS MSB								LSB	ANALOG OUTPUT
1	1	1	1		1	1	1	1	$+V_{REF}\left(\frac{127}{128}\right)$
1	0	0	0		0	0	0	1	$+V_{REF}\left(\frac{1}{128}\right)$
1	0	0	0		0	0	0	0	0V
0	1	1	1		1	1	1	1	$-V_{REF}\left(\frac{1}{128}\right)$
0	0	0	0		0	0	0	1	$-V_{REF}\left(\frac{127}{128}\right)$
0	0	0	0		0	0	0	0	$-V_{REF}\left(\frac{128}{128}\right) = -V_{REF}$

Note: 1 LSB = $(V_{REF})(2^{-8}) = +V_{REF}\left(\frac{1}{256}\right)$

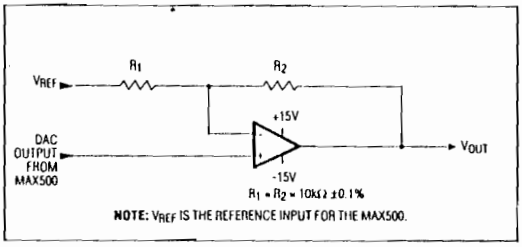


Figure 9. Bipolar Output Circuit

Offsetting AGND

AGND can be biased above DGND to provide an arbitrary nonzero output voltage for a "zero" input code. This is shown in Figure 10. The output voltage at $V_{OUT}A$ is:

$$V_{OUT}A = V_{BIAS} + D_AV_{IN}$$

where D_A is a fractional representation of the digital input word. Since AGND is common to all four DACs, all outputs will be offset by V_{BIAS} in the same manner. Since AGND current is a function of the 4 DAC codes, it should be driven by a low impedance source. V_{BIAS} must be positive.

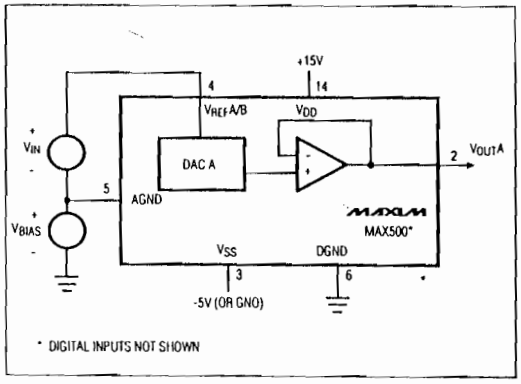


Figure 10. AGND Bias Circuit

Using an AC Reference

In applications where V_{REF} has AC signal components, the MAX500 has multiplying capability within the limits of the V_{REF} input range specifications. Figure 11 shows a technique for applying a sine wave signal to the reference input where the AC signal is biased up before being applied to V_{REF}. Output distortion is typically less than 0.1% with input frequencies up to 50kHz, and the typical -3dB frequency is 700kHz. Note that V_{REF} must never be more negative than AGND.

CMOS Quad, Serial Interface, 8-Bit D/A Converter

Generating Vss

The performance of the MAX500 is specified for both dual and single supply (V_{SS} = 0V) operation. When the improved performance of dual supply operation is desired, but only a single supply is available, a -5V V_{SS} supply can be generated using an ICL7660 in one of the circuits of Figure 12.

Digital Interface Applications

Figures 13 through 16 show examples of interfacing the MAX500 to most popular microprocessors.

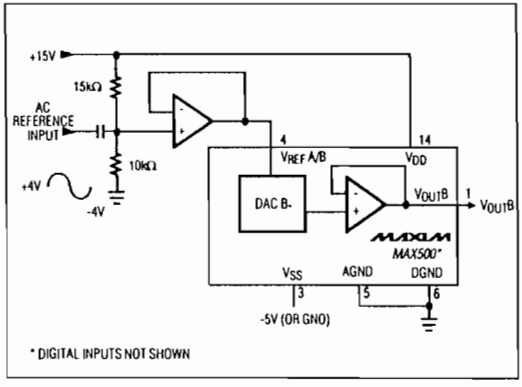


Figure 11. AC Reference Input Circuit

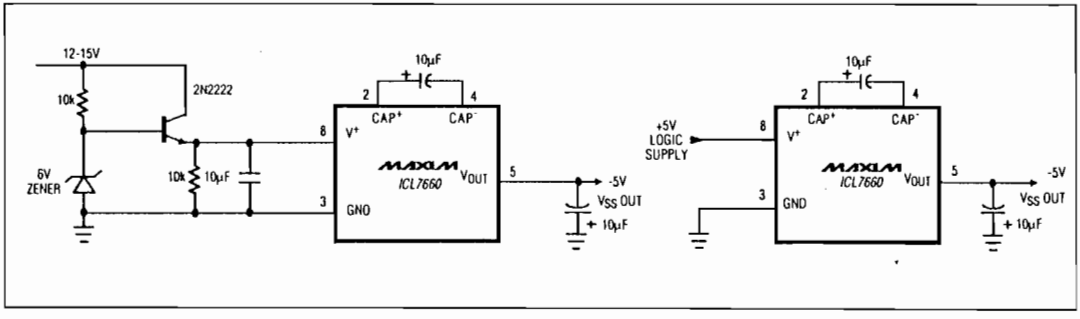


Figure 12. Generating -5V for V_{SS}

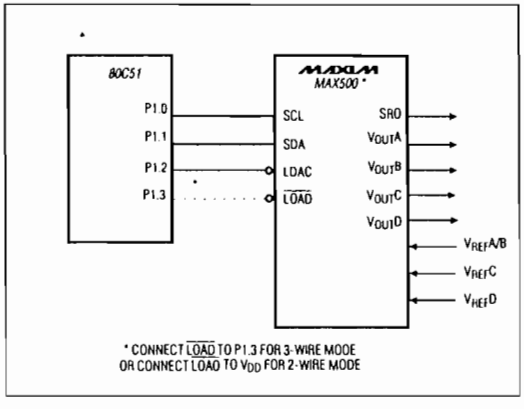


Figure 13. 80C51 Interface

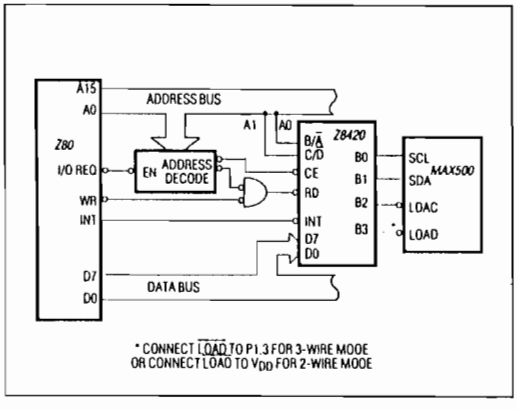


Figure 14. Z-80 with Z8420 PIO Interface

CMOS Quad, Serial Interface, 8-Bit D/A Converter

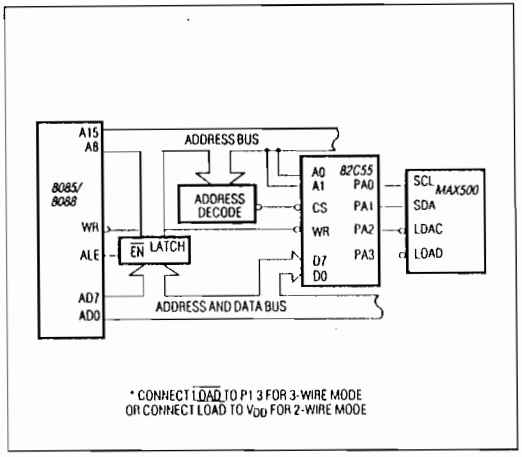


Figure 15. 8085/8088 with Programmable Peripheral Interface

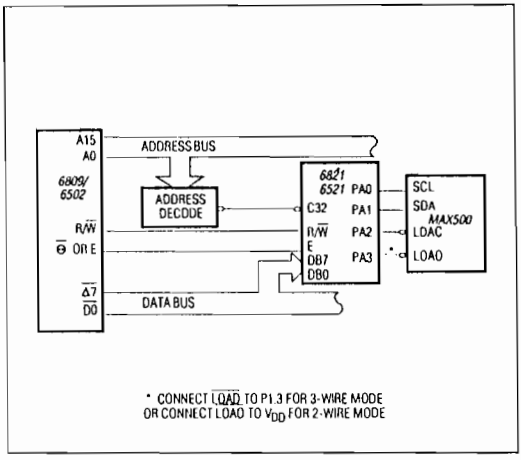
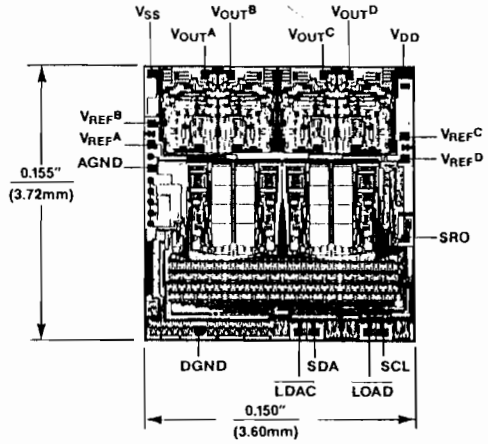


Figure 16. 6809/6502 Interface

Chip Topography



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